**WHAT IS CLAIMED IS:**

1. A semiconductor device, comprising:

a recrystallized polysilicon layer located over a gate electrode layer; and

a capacitor located on said recrystallized polysilicon layer, said capacitor, including;

a first electrode;

an insulator located over said first electrode; and

a second electrode located over said insulator.

2. The semiconductor device as recited in Claim 1 wherein said first electrode comprises a silicide.

3. The semiconductor device as recited in Claim 2 wherein said first electrode comprises cobalt silicide.

4. The semiconductor device as recited in Claim 1 wherein said first electrode has a surface roughness ranging from about 1 nm to about 2 nm.

5. The semiconductor device as recited in Claim 1 wherein at least a portion of said recrystallized polysilicon layer forms a portion of said first electrode.

6. The semiconductor device as recited in Claim 1 wherein said recrystallized polysilicon layer has a final thickness ranging from about 7 nm to about 35 nm.

7. The semiconductor device as recited in Claim 1 wherein said gate electrode layer is a polysilicon layer and said recrystallized polysilicon layer is located on said polysilicon layer.

8. The semiconductor device as recited in Claim 7 wherein said polysilicon layer and said recrystallized polysilicon layer form at least a portion of a gate electrode stack.

9. A method for manufacturing a semiconductor device, comprising:

forming an amorphous silicon layer over a substrate;

changing said amorphous silicon layer to a recrystallized polysilicon layer; and

creating a capacitor on said recrystallized polysilicon layer, said capacitor including;

a first electrode;

an insulator located over said first electrode;

a second electrode located over said insulator.

10. The method as recited in Claim 9 wherein forming an amorphous silicon layer includes depositing an amorphous silicon layer having a thickness ranging from about 15 nm to about 75 nm.

11. The method as recited in Claim 9 wherein changing said amorphous silicon layer to a recrystallized polysilicon layer includes subjecting said amorphous silicon layer to an annealing process, said annealing process causing said amorphous silicon layer to become said recrystallized polysilicon layer.

12. The method as recited in Claim 11 wherein subjecting said amorphous silicon layer to an annealing process includes subjecting said amorphous silicon layer to a temperature ranging from about 1000°C to about 1100°C.

13. The method as recited in Claim 9 wherein forming an amorphous silicon layer over a substrate includes forming an amorphous silicon layer on a polysilicon layer, wherein said amorphous silicon layer and said polysilicon layer form at least a part of a gate electrode stack.

14. The method as recited in Claim 13 wherein said amorphous silicon layer has a thickness ranging from about 15 nm to about 75 nm and said polysilicon layer has a thickness ranging from about 50 nm to about 150 nm.

14. The method as recited in Claim 9 wherein creating a capacitor first electrode includes creating a capacitor first electrode comprising a silicide.

15. The method as recited in Claim 14 wherein said silicide comprises cobalt silicide.

16. The method as recited in Claim 9 wherein creating a capacitor first electrode includes creating a capacitor first electrode having a surface roughness ranging from about 1 nm to about 2 nm.

17. The method as recited in Claim 9 wherein creating a capacitor first electrode includes creating a capacitor first electrode having a thickness ranging from about 15 nm to about 70 nm.

18. An integrated circuit, comprising:

transistors located over a substrate, wherein at least one of said transistors includes a gate electrode stack comprising a recrystallized polysilicon layer located over a gate electrode layer;

a capacitor located on said recrystallized polysilicon layer, said capacitor including;

a first electrode;

an insulator located over said first electrode; and

a second electrode located over said insulator; and

an interlevel dielectric layer located over said substrate, said interlevel dielectric layer having interconnects located therein for contacting at least one of said gate electrode stack or said capacitor.

19. The integrated circuit as recited in Claim 18 wherein at least a portion of said recrystallized polysilicon layer forms a portion of said first electrode.

20. The integrated circuit as recited in Claim 18 wherein said transistors are selected from the group consisting of:

a CMOS transistor;

a bipolar transistor; and

a biCMOS transistor.